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IN THE U.S. PATENT AND TRADEMARK OFFICE

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In re Application of
Watts
Serial No.: 08/568,904
Filed: 12/07/95
For: REAL-TIME THERMAL MANAGEMENT FOR COMPUTERS

TI-20567
Art Unit: 2781
Examiner: Dharia

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APPEAL BRIEF TRANSMITTAL FORM

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

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Elizabeth Austin — Date 3/25/99

Transmitted herewith in triplicate is an Appellant's Brief in the above-identified application.

Charge any additional fees, or credit overpayment to Deposit Account No. 20-0668. An original and two copies of this sheet are enclosed.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
Watts
Serial No.: 08/568,904
Filed: 12/07/95
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APPELLANT'S BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

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Ronald O. Neerings, Reg. No. 34227

Dear Sir:

In support of his appeal of the Rejection of claims in the above-referenced application, Appellant respectfully submits herein his brief.

I. REAL PARTY IN INTEREST

Texas Instruments Incorporated is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals or interferences.

III. STATUS OF CLAIMS

Claims 2-3, 5-6, 9, 17-21, 23, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 are pending in the application. Final Rejection of Claims 2-3, 5-6, 9, 17-21, 23, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 was made by the Examiner in an Office Action dated October 14, 1998. Claims 2-3, 5-6, 9, 17-21, 23, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 are on appeal. Claims 2-3, 5-6, 9, 17-21, 23, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 are reproduced in the Appendix to Appellant's Brief filed herewith.

IV. STATUS OF AMENDMENTS

Appellant's last amendment was an amendment under 37 C.F.R. 1.115 dated July 28, 1998, which was entered by the Examiner. No subsequent amendments have been filed.

V. SUMMARY OF THE INVENTION

In one embodiment of the invention, Appellant discloses an apparatus comprising: "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "a monitor for monitoring temperature within said apparatus", and "a clock manager adapted to receive a control signal from said monitor, said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level and said CPU is not processing critical I/O".

In another embodiment of the invention, Appellant discloses an apparatus comprising: "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed" and "a clock manager coupled to a monitor that monitors temperature within said apparatus, said clock manager designating that

said central processing unit (CPU) receives said first clock signal when said monitored temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level and said CPU is not processing critical I/O."

In yet another embodiment of the invention, Appellant discloses an apparatus comprising: "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "a monitor for monitoring temperature within said apparatus" and "a clock manager adapted to receive a control signal from said monitor, said clock manager reducing central processing unit (CPU) clock speed when a detected temperature level is at and above a selected reference temperature level and said CPU is not processing critical I/O".

VI. ISSUES

1) Are Claims 2-3, 5-6, 9, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 patentable under 35 U.S.C. §103 over Hollowell, II et al. In view of Kikinis and further in view of Gephardt et al?

2) Are Claims 17-21 and 23 patentable under 35 U.S.C. §103(a) over Hollowell, II et al in view of Kikinis and further in view of Chen et al?

VII. GROUPING OF CLAIMS

Claims 2, 3, 5, 6, 9, 17-21, 23, 30, 31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 stand or fall separately.

VIII. ARGUMENT

The Rejection

Claims 2-3, 5-6, 9, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 are rejected under 35 U.S.C. § 103 as being unpatentable over Hollowell, II et al. in view of Kikinis and further in view of Gephardt et al.

As per claims 2, 3, 5, and 9, Hollowell discloses the claimed invention including a provision for user input (Fig. 1); a provision for output (Fig. 1); a CPU coupled to the input and output (Fig. 1; col. 4, lines 6-7); the input is a keyboard (Fig. 1; col. 4, lines 42-44); the output is a display device (Fig. 1; col. 4, lines 21-22); a temperature level detector (Fig. 1; col. 4, lines 47-48); and a thermal management system that stops the power to the CPU when the temperature detected exceeds a reference temperature (Abstract; Fig. 2). However, Hollowell does not teach stopping the clock signals when a detected temperature rises above a reference temperature level. Kikinis teaches a system for controlling temperature buildup in an IC which employs a temperature sensor to provide an indication of the IC temperature to a control circuit which is configured to adjust the clock speed based upon a function of the temperature of the IC or its package (Abstract). Further, Kikinis teaches that it is known to selectively stop clock signals when the detected temperature rises above a reference temperature level (Abstract; Fig. 3, 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the selectively stopping the clock signals based upon rising temperatures exceeding a reference temperature as taught by Kikinis, to monitor the temperature levels in the computer, to prevent excessive temperature which may damage vital components or circuitry.

Hollowell and Kikinis disclose the claimed invention as discussed above. However, Hollowell does not teach a monitor stopping the clock signals to the CPU only when the CPU is not processing critical I/0. Gephardt teaches a power management that monitors CPU activity and dependent upon the type of activity, controls the frequencies of the CPU clock signal and system clock signal (Abstract; Fig. 6). Furthermore, Gephardt teaches the clock signals be raised if certain system activities are detected and to be lowered if certain other activities are detected

(col. 2, lines 23-32, lines 64-67; col. 3, lines 1-34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to stop the clock only when the CPU is processing non-critical I/0 as taught by Gephardt, to prevent losing any vital information or processing that may occur during an I/0 operation.

As per claim 6, Hollowell, Kikinis and Gephardt disclose the claimed invention as discussed above. However, Hollowell does not teach a CPU receiving a one of a first clock signal at a first speed or a second clock signal at a second speed and the CPU receives the first clock signal when the temperature is below the reference temperature and the receives the second clock signal when the temperature is greater than or equal to the reference temperature. Kikinis teaches that it is known to provide first and second clock signals with first and second speeds to the CPU (col. 4, lines 23-53). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Kikinis, to provide different clock speeds based upon the required load of the CPU.

As per claims 30 and 31, Hollowell and Kikinis disclose the claimed invention as described in the above claims. However, Hollowell and Kikinis do not teach the clock manager stops clock signals from being sent to a PCI bus coupled to the CPU or any other CPUs coupled to the PCI bus. Gephardt teaches that the above features are well known (Fig. 2, col. 11, lines 13-21). It would have been obvious to one of ordinary skill. in the art at the time the invention was made to include the above features, as taught by Gephardt to more efficiently conserve power by managing power also to external devices.

As per claims 33-39, Hollowell, Kikinis, and Gephardt disclose the claimed invention as described above. However, Hollowell does not teach the monitor is on board the CPU and the monitor detects via a temperature sensor. Kikinis teaches that it is known to have a monitor on the board with the CPU and the monitor detects via a temperature sensor (Fig. 2, 3, col. 3, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the above features as taught by Kikinis, to provide an accurate and efficient way to measure temperature.

As per claims 41-43, 45-47, and 49-51, Hollowell, Kikinis, and Gephardt disclose the claimed invention as described above. Furthermore, Hollowell and Kikinis teach that the temperature sensor is located on the CPU board (Fig. 1) or on the CPU (Fig. 3). The location of the temperature sensor is dependent upon the area of concern. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the temperature sensor as taught by Hollowell and Kikinis to provide the system designer the freedom to measure in close proximity to area of temperature concern.

As per claim 53-55, Hollowell, Kikinis and Gephardt disclose the claimed invention as described above. Furthermore, Hollowell teaches the temperature sensing device may be a thermistor (col. 6, lines 31-33).

As per claim 57-59, Hollowell, Kikinis and Gephardt disclose the claimed invention as described above. Furthermore, Hollowell teaches the temperature sensing is monitored periodically (col. 6, lines 46-47).

As per claim 61-63, Hollowell, Kikinis and Gephardt disclose the claimed invention as described above. Furthermore, Hollowell teaches the frequency of temperature sensing changes as the temperature reaches a preselected threshold value (col. 7, lines 44
50).

As per claim 65-67, Hollowell, Kikinis and Gephardt disclose the claimed invention as described above. However, Hollowell does not teach that the temperature sensing is user modifiable. Kikinis teaches that it is known for the temperature sensing to be user modifiable (col. 5, lines 64-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the user modifiable temperature sensing as taught by Kikinis to give the user the flexibility to adjust the temperature sensing for testing purposes.

As per claim 71-73, Hollowell, Kikinis and Gephardt disclose the claimed invention as described above. However, Hollowell does not teach the monitor uses a control system of continuous feedback loops. Kikinis teaches that it is known to use a control system of

continuous feedback loops (Fig. 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the continuous feedback loops as taught by Kikinis, to maintain and regulate the temperature in the IC to prevent large temperature swings which causes excess power and could cause physical damage to the components.

Claims 17-21, and 23, are rejected under 35 U. S.C. 103(a) as being unpatentable over Hollowell, II et al in view of Kikinis and further in view of Chen et al.

As per claims 17, 18 and 21, Hollowell and Kikinis disclose the claimed invention including monitoring temperature levels in a computer. However, Hollowell and Kikinis do not teach predicting activity and temperature levels relevant to the operation of a CPU within the computer and using the predictions for automatic temperature control. Chen teaches that it is known to predict activity levels within a computer and using the prediction for automatic control and also, remain transparent to the user (col. 7, lines 4-24). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Chen, since having the capability to predict temperature rises and automatically control them, prior to the occurrence could prevent premature failure of the CPU or circuit components.
As per claims 19, 20, and 23, Hollowell and Kikinis teach the disclosed invention as claims 17, 18, and 23 above. However, Hollowell and Kikinis do not teach user modification of automatic activity and temperature level predictions and using modified predictions for automatic temperature control. Chen teaches that it is known to allow user modification of automatic activity level predictions and using the modified predictions for automatic control (col. 7, lines 5-43, col. 8, lines 1-6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Chen, since allowing the user to modify temperature levels would allow for different manufacturer's components that have various temperature specifications.

Appellant's Argument

1) Claims 2-3, 5-6, 9, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 are allowable under 35 U.S.C. §103 over Hollowell, II et al. in view of Kikinis and

further in view of Gephardt et al.

Independent Claim 5 requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "**a monitor for monitoring temperature within said apparatus**", and "**a clock manager adapted to receive a control signal from said monitor, said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level and said CPU is not processing critical I/O**".

Independent Claim 6, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed" and "**a clock manager coupled to a monitor that monitors temperature within said apparatus, said clock manager designating that said central processing unit (CPU) receives said first clock signal when said monitored temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level and said CPU is not processing critical I/O.**"

Independent Claim 9, as amended, requires and positively recites, "a provision for user input", "a provision for output", "a central processing unit (CPU) coupled to said user input and output", "**a monitor for monitoring temperature within said apparatus**" and "**a clock manager adapted to receive a control signal from said monitor, said clock manager reducing central processing unit (CPU) clock speed when said detected temperature level is at and above a selected reference temperature level and said CPU is not processing critical I/O**".

Appellant agrees with the Examiner's analysis of Hollowell as set forth in the Office Action dated April 28, 1998 (page 3, line 3 – page 4, line 6). Appellant also agrees with the Examiner that Hollowell does not teach stopping the clock signals when a detected temperature

rises above a reference temperature level (page 4, lines 4-6). Appellant further agrees with the Examiner that Hollowell does not teach a monitor stopping the clock signals to the CPU only when the CPU is processing non-critical I/O (page 4, lines 16-18).

While Kikinis teaches that it is known to selectively stop clock signals when the detected temperature rises above a reference temperature level, Kikinis fails to teach or suggest that the selective stopping is performed only when the monitored temperature is **at or above** a selected reference **and said CPU is not processing critical I/O**. Moreover, Kikinis fails to teach or suggest any modification of the clock signal to the processor for any reasons other than temperature. Indeed, the Kikinis and Hollowell references, alone or in combination, fail to teach or suggest that critical I/O will, or should, affect the performance of the temperature reduction mechanism.

Gephardt is the reference newly combined with Hollowell and Kikinis. Gephardt teaches, in the Background of the Invention:

> Although a variety of prior art system have been proposed in which the power management unit causes the frequencies of selected clock signals to be raised if certain system activities are detected and to be lowered if other system activities are not detected, **such systems typically do not treat the detected activities differently. As a result, the efficiency of these systems may be somewhat limited since many detected activities have different associated impacts upon power consumption** (col. 2, lines 23-31)(emphasis added).

Assuming, arguendo, that Gephardt teaches a power management architecture that monitors CPU activity and, dependent upon one of the classifications of activity being detected on table II (col. 9, lines 14-25), can control the frequency of the CPU clock signal and system clock signal as suggested by the Examiner, Gephardt fails to teach or suggest any means for detecting "critical activity". Moreover, fails to mention "critical activity" at all in any context. Furthermore, to the extent that "activity" is defined in Gephardt, it never associates "temperature" with an "activity" classification.

Further, Gephardt teaches that clock speed is decreased in response to reduced levels of activity – thus lower clock speed for lower level of activity – and higher levels of speed for

higher levels of activity. In contrast, the present invention stops (or reduces) clock speed "when said clock speed rises to a level at and above a selected reference temperature level and said CPU is not processing critical I/O". It would not have been obvious to one having ordinary skill in the art at the time the invention was made to combine Gephardt with Kikinis and Hollowell and modify the resulting device so that the resulting temperature reduction mechanism will selectively stop (or reduce) the clock signal to the CPU only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)). The Examiner has not met this burden in the present case. The Examiner has not provided any evidence of knowledge generally available to one of ordinary skill in the art at the time of the invention that would lead that individual to combine the relevant teachings of the Kikinis, Hollowell and Gephardt references. Moreover, even if there were such teaching, the Examiner provides no teaching or suggestion, without the improper hindsight provided by Appellant's disclosure, for the additional modifications that would be required by any combination device in order for it to be able to obviate the claimed invention.

Even if the cited art were to disclose components of the device in issue, case law holds that it is insufficient that the prior art discloses the components of the device in issue, either separately or used in other combination; there must be some teaching, suggestion, or incentive to make the combination made by the inventor. Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934, 15 USPQ2d 1321, 1323 (Fed. Cir. 1990). Moreover, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of

references can be combined ONLY if there is some suggestion or incentive to do so." ACS Hosp. Systems, Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The Examiner in the present case has not provided any teaching or suggestion from the art supporting the combination.

Moreover, the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Simply put, the prior art does not teach or suggest the modifications necessary to attain Appellant's claimed invention. Accordingly, the Examiner has improperly used hindsight and Appellant's disclosure to obviate his claimed invention. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). Moreover, "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). The 35 U.S.C. §103 rejection is overcome. Just because something is desirable (especially in hindsight) does not mean it is obvious.

Claims 2, 3, 30-31, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the apparatus of Claim 5 wherein said user input is coupled to a keyboard. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 3 further defines the apparatus of Claim 5 wherein said output is coupled to a display device. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 30 further defines the apparatus of Claim 5, wherein said clock manager further stops clock signals from being sent to a PCI bus coupled to the central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5. While Gehpardt discloses that "power management unit 208 of FIG. 2 controls the generation of various clock signals with computer system 200 ... and power management unit 208 may be configured to control only selected clock signals of computer system 200" (col. 11, lines 15-19), it does not teach or suggest, a clock manager further stopping clock signals from being sent to a PCI bus coupled to the central processing unit (CPU).

Claim 31 further defines the apparatus of Claim 30 wherein said clock manager further stops clock signals from being sent to any other CPUs connected to the PCI bus. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5. While Gehpardt discloses that "power management unit 208 of FIG. 2 controls the generation of various clock signals with computer system 200 ... and power management unit 208 may be configured to control only selected clock signals of computer system 200" (col. 11, lines 15-19), it does not teach or suggest, a clock manager further stopping clock signals from being sent to any other CPUs connected to the PCI bus.

Claim 34 further defines the apparatus of Claim 5, wherein said monitor is on board said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 35 further defines the apparatus of Claim 9, wherein said monitor is on board said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 9.

Claim 36 further defines the apparatus of Claim 6, wherein said monitor is on board said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 37 further defines the apparatus of Claim 6, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU). In Kikinis and Hollowell, the temperature sensor is coupled to a microcontroller, NOT a central processing unit (CPU). As a result, the Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 38 further defines the apparatus of Claim 5, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).). In Kikinis and Hollowell, the temperature sensor is coupled to a microcontroller, NOT a central processing unit (CPU). As a result, the Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 39 further defines the apparatus of Claims 9, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).). In Kikinis and Hollowell, the temperature sensor is coupled to a microcontroller, NOT a central processing unit (CPU). As a result, the Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 9.

Claim 41 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted directly on said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 42 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted directly on said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 43 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted directly on said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 39.

Claim 45 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted within said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 46 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted within said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 38.

Claim 47 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted within said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 39.

Claim 49 further defines the apparatus of Claim 37, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 50 further defines the apparatus of Claim 38, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 38.

Claim 51 further defines the apparatus of Claim 39, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 53 further defines the apparatus of Claim 37, wherein said temperature sensor is a thermistor. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 37.

Claim 54 further defines the apparatus of Claim 38, wherein said temperature sensor is a thermistor. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 38.

Claim 55 further defines the apparatus of Claim 39, wherein said temperature sensor is a thermistor. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 39.

Claim 57 further defines the apparatus of Claim 6, wherein said temperature is sensed on a periodic basis. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 58 further defines the apparatus of Claim 5, wherein said temperature is sensed on a periodic basis. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 59 further defines the apparatus of Claim 9, wherein said temperature is sensed on a periodic basis. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 61 further defines the apparatus of Claim 57, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 57.

Claim 62 further defines the apparatus of Claim 58, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 58.

Claim 63 further defines the apparatus of Claim 59, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 59.

Claim 65 further defines the apparatus of Claim 57, wherein the frequency of said temperature sensing is user modifiable. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 57.

Claim 66 further defines the apparatus of Claim 58, wherein the frequency of said temperature sensing is user modifiable. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 58.

Claim 67 further defines the apparatus of Claim 59, wherein the frequency of said temperature sensing is user modifiable. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 59.

Claim 71 further defines the apparatus of Claim 11, wherein said monitor uses a control system of continuous feedback loops. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 11.

Claim 72 further defines the apparatus of Claim 5, wherein said monitor uses a control system of continuous feedback loops. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 5.

Claim 73 further defines the apparatus of Claim 9, wherein said monitor uses a control system of continuous feedback loops. The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 9.

2) Claims 17-21 and 23 are allowable under 35 U.S.C. 103(a) over Hollowell, et al in view of Kikinis and further in view of Chen et al.

Independent 17, as amended, requires and positively recites, "means for sampling a temperature level associated with the operation of a central processing unit within said computer", "**means for predicting temperature levels associated with the operation of said central processing unit within said computer**" and "**means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer**".

Independent Claim 18, as amended, requires and positively recites, "means for sampling a temperature level associated with the operation of said computer", "**means for predicting temperature levels associated with the operation of said computer**" and "**means for using said prediction for automatic temperature control within said computer, said temperature control remaining transparent to a user of said computer**".

Appellant agrees with the Examiner that Hollowell and Kikinis "do not teach predicting temperature levels relevant to the operation of a CPU within the computer and using the predictions for automatic temperature control" (Office Action dated April 28, 1998 (page 8, lines 4–6). Appellant also agrees with the Examiner that Hollowell does not teach stopping the clock signals when a detected temperature rises above a reference temperature level (page 4, lines 4-6) and does not teach a monitor stopping the clock signals to the CPU only when the CPU is processing non-critical I/O (page 4, lines 16-18).

The Chen reference teaches a temperature control system which employs feedback to adjust the output count signal (col. 2, lines 43-44) in which NO TEMPERATURE MEASUREMENTS ARE NEEDED OR MADE (col. 2, lines 44-45). Appellant respectfully traverses the Examiner's statement that Chen teaches that "it is known to predict activity and temperature levels relevant to the operation of a CPU within the computer using the predictions for automatic temperature control" (Office Action dated October 14, 1998, page 7, lines 6-8). Chen specifically states, "determining a piecewise **estimate of CPU temperature change** as a function of time over an accumulated operating history of the CPU" (col. 7, lines 8-10)". Thus, Chen makes a piecewise ESTIMATE of CPU temperature CHANGE. It does not teach or suggest, "**means for predicting temperature levels associated with the operation of said central processing unit within said computer**" and "**means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer**", as required by Claim 17, or "**means for predicting temperature levels associated with the operation of said computer**" and "**means for using said prediction for automatic temperature control within said computer, said temperature control remaining transparent to a user of said computer**", as required by Claim 18.

Thus, it would not be obvious to one of ordinary skill in the art without improper hindsight to combine the teachings of Chen with Hollowell and Kikinis, and thereafter modify the resulting apparatus to be an apparatus that both samples the temperature within the computer (or CPU) and there after uses the temperature sample in predicting temperature levels associated with the operation of a computer (or CPU).

As a result, any combination of the Hollowell, Kikinis and Chen references fails to teach or suggest, "means for sampling a temperature level associated with the operation of a central processing unit within said computer", "means for predicting temperature levels associated with the operation of said central processing unit within said computer" and "means for using said prediction for automatic control of temperature within said computer", as required by Claim 17, or "means for sampling a temperature level associated with the operation of said computer", "means for predicting temperature levels associated with the operation of said computer" and "means for using said prediction for automatic temperature control within said computer", as required by Claim 18.

Independent Claim 21 requires and positively recites, "a central processing unit (CPU)", "means for sampling a temperature level within said apparatus" and "**means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal utilized by the central processing unit (CPU) to maintain said temperature level within said apparatus below a selected reference temperature level when said CPU is not processing critical I/O**".

As stated above, Chen teaches a temperature prediction mode in which in which NO TEMPERATURE MEASUREMENTS ARE NEEDED OR MADE (col. 2, lines 44-45).. Kikinis, on the other hand, discloses a device in which temperature measurements ARE MADE – i.e., which selectively stops clock signals when the detected temperature rises above a reference temperature level. Kikinis fails, however, to teach or suggest that the selective stopping be performed only when the monitored temperature is at or above a selected reference and said CPU is not processing critical I/O. Kikinis also fails to teach or suggest any modification of the clock signal to the processor for any reasons other than temperature. Any combination of Chen,

Kikinis and Hollowell, fails to address the discrepancies between, or justify any combination of the Chen and Kikinis (regarding temperature measurements and temperature prediction) with the Hollowell reference. Moreover, none of the references (alone or in combination) teach or suggest that critical I/O will, or should, affect the performance of the temperature reduction mechanism.

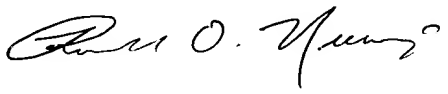
As stated previously, the mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Simply put, the prior art does not teach or suggest the modifications necessary to attain Appellant's claimed invention. Accordingly, the Examiner has improperly used hindsight and Appellant's disclosure to obviate his claimed invention. It is also impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). Moreover, "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). The 35 U.S.C. §103 rejection is overcome.

Claim 23 further defines the apparatus of Claim 21, wherein said adjustments are accomplished within the central processing unit (CPU) cycles and do not affect the user's perception of performance. The Kikinis and Chen references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 21.

Claims 2, 3, 5, 6, 9, 11, 16-19, 34-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67 and 71-73 stand allowable and the application is in allowable form.

For the above reasons, favorable consideration of the appeal of the Final Rejection in the above-referenced application, and its reversal, are respectfully requested.

Respectfully submitted,



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APPENDIX

CLAIMS ON APPEAL

2. The apparatus of Claim 5, wherein said user input is coupled to a keyboard.

3. The apparatus of Claim 5, wherein said output is coupled to a display device.

5. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a monitor for monitoring temperature within said apparatus; and

a clock manager adapted to receive a control signal from said monitor, said clock manager selectively stopping clock signals from being sent to said central processing unit (CPU) when said monitored temperature rises to a level at and above a selected reference temperature level and said CPU is not processing critical I/O.

6. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output, said central processing unit (CPU) receiving one of a first clock signal at a first speed or a second clock signal at a second speed; and

a clock manager coupled to a monitor that monitors temperature within said apparatus, said clock manager designating that said central processing unit (CPU) receives said first clock signal when said monitored temperature is at a level below a selected reference temperature level and receives said second clock signal when said detected temperature is at a level at and above said selected reference temperature level and said PCU is not processing critical I/O.

9. An apparatus, comprising:

a provision for user input;

a provision for output;

a central processing unit (CPU) coupled to said user input and output;

a monitor for monitoring temperature within said apparatus; and

a clock manager adapted to receive a control signal from said monitor, said clock manager reducing central processing unit (CPU) clock speed when a detected temperature level is at and above a selected reference temperature level and said CPU is not processing critical I/O.

17. A computer, comprising:

means for sampling a temperature level associated with the operation of a central processing unit within said computer;

means for predicting temperature levels associated with the operation of a central processing unit within said computer; and

means for using said prediction for automatic control of temperature within said computer, said temperature control remaining transparent to a user of said computer.

18. A computer, comprising:

means for sampling a temperature level associated with the operation of said computer;

means for predicting temperature levels associated with the operation of said computer; and

means for using said prediction for automatic temperature control within said computer, said temperature control remaining transparent to a user of said computer.

19. The computer of Claim 17, including means for user modification of said temperature level predictions.

20. The computer of Claim 18, including means for user modification of said temperature level predictions.

21. An apparatus, comprising:

a central processing unit (CPU);

means for sampling a temperature level within said apparatus; and

means for automatically adjusting the processing speed of said central processing unit (CPU) by modifying the clock signal utilized by the central processing unit (CPU) to maintain said temperature level within said apparatus below a selected reference temperature level when said CPU is not processing critical I/O.

23. The apparatus of Claim 21, wherein said adjustments are accomplished within the central processing unit (CPU) cycles and do not affect the user's perception of performance.

30. The apparatus of Claim 5 wherein said clock manager further stops clock signals from being sent to a PCI bus coupled to the central processing unit (CPU).

31. The apparatus of Claim 30 wherein said clock manager further stops clock signals from being sent to any other CPUs connected to the PCI bus.

34. The apparatus of Claim 5, wherein said monitor is on board said central processing unit (CPU).

35. The apparatus of Claim 9, wherein said monitor is on board said central processing unit (CPU).

36. The apparatus of Claim 6, wherein said monitor is on board said central processing unit (CPU).

37. The apparatus of Claim 6, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

38. The apparatus of Claim 5, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

39. The apparatus of Claims 9, wherein said monitored temperature is detected via a temperature sensor coupled to said central processing unit (CPU).

41. The apparatus of Claim 37, wherein said temperature sensor is mounted directly on said central processing unit (CPU).

42. The apparatus of Claim 38, wherein said temperature sensor is mounted directly on said central processing unit (CPU).

43. The apparatus of Claim 39, wherein said temperature sensor is mounted directly on said central processing unit (CPU). The Hollowell, Kikinis, and Gephardt references fail, alone or in combination, to teach or suggest this further limitation in combination with the requirements of Claim 39.

45. The apparatus of Claim 37, wherein said temperature sensor is mounted within said central processing unit (CPU).

46. The apparatus of Claim 38, wherein said temperature sensor is mounted within said central processing unit (CPU).

47. The apparatus of Claim 39, wherein said temperature sensor is mounted within said central processing unit (CPU).

49. The apparatus of Claim 37, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU).

50. The apparatus of Claim 38, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU).

51. The apparatus of Claim 39, wherein said temperature sensor is mounted on a printed wiring board (PWB) adjacent said central processing unit (CPU).

53. The apparatus of Claim 37, wherein said temperature sensor is a thermistor..

54. The apparatus of Claim 38, wherein said temperature sensor is a thermistor. .

55. The apparatus of Claim 39, wherein said temperature sensor is a thermistor.

57. The apparatus of Claim 6, wherein said temperature is sensed on a periodic basis.

58. The apparatus of Claim 5, wherein said temperature is sensed on a periodic basis.

59. The apparatus of Claim 9, wherein said temperature is sensed on a periodic basis.

61. The apparatus of Claim 57, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values.

62. The apparatus of Claim 58, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values.

63. The apparatus of Claim 59, wherein the frequency of said temperature sensing changes as said temperature reaches preselected threshold values.

65. The apparatus of Claim 57, wherein the frequency of said temperature sensing is user modifiable.

66. The apparatus of Claim 58, wherein the frequency of said temperature sensing is user modifiable.

67. The apparatus of Claim 59, wherein the frequency of said temperature sensing is user modifiable.

71. The apparatus of Claim 6, wherein said monitor uses a control system of continuous feedback loops.

72. The apparatus of Claim 5, wherein said monitor uses a control system of continuous feedback loops.

73. The apparatus of Claim 9, wherein said monitor uses a control system of continuous feedback loops.